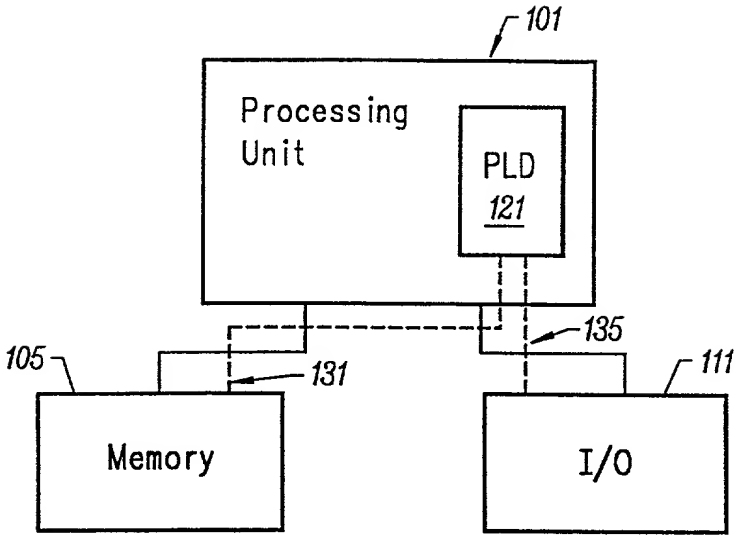


FIGURE 1

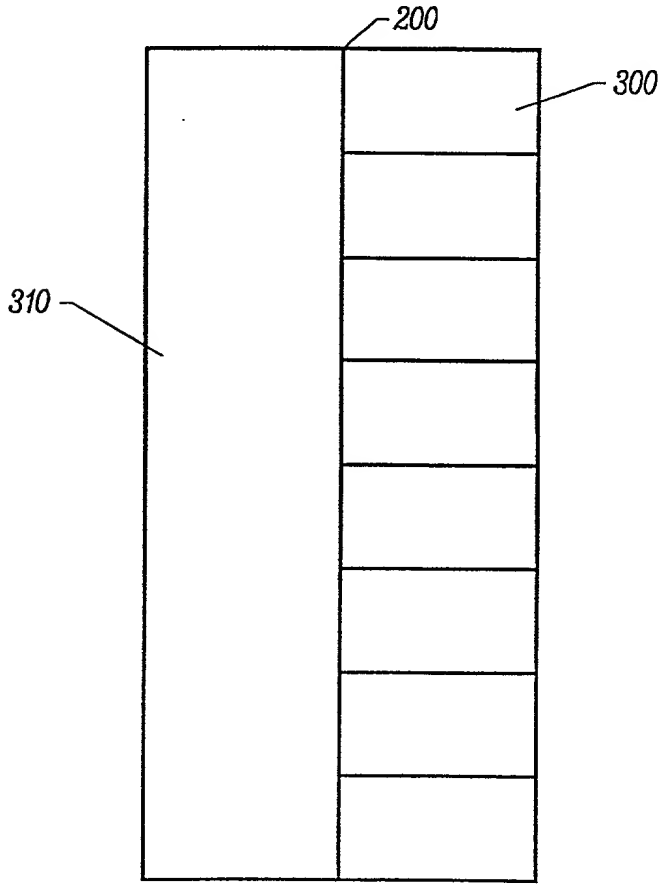
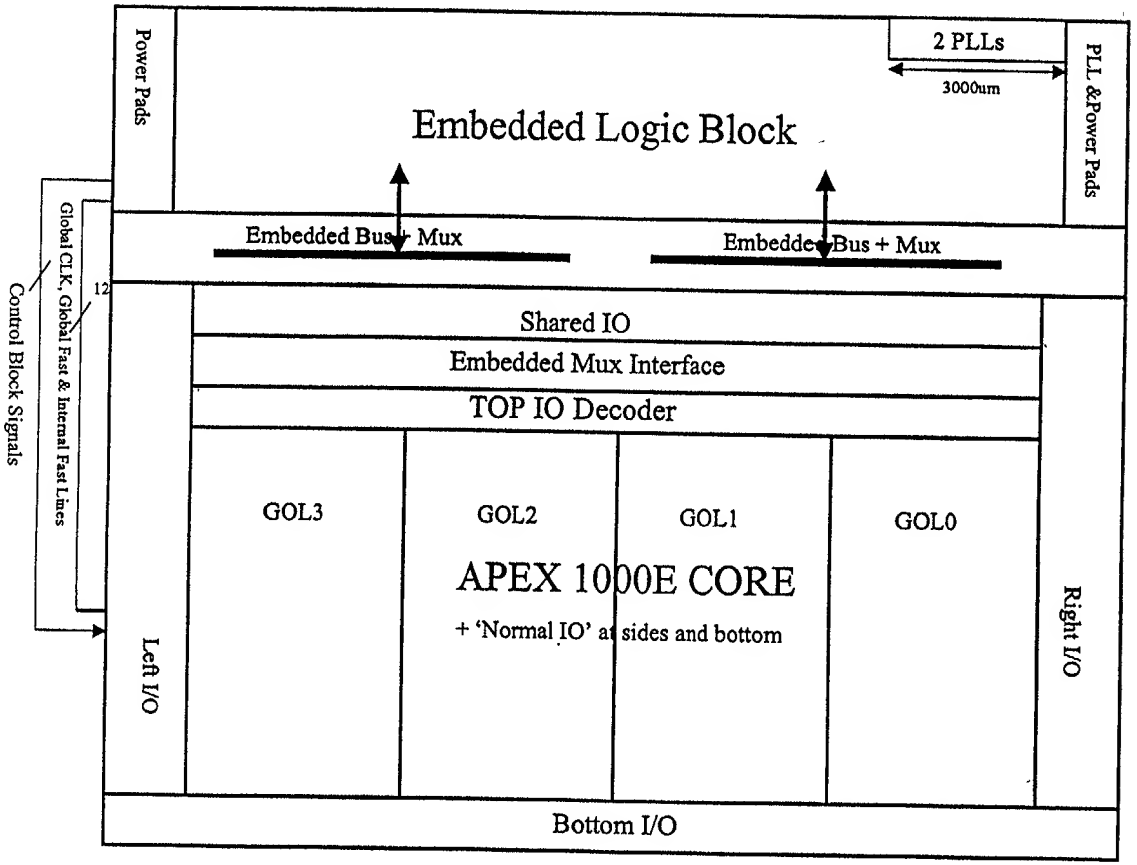


FIGURE 4



Top Level Floorplan

FIGURE 2

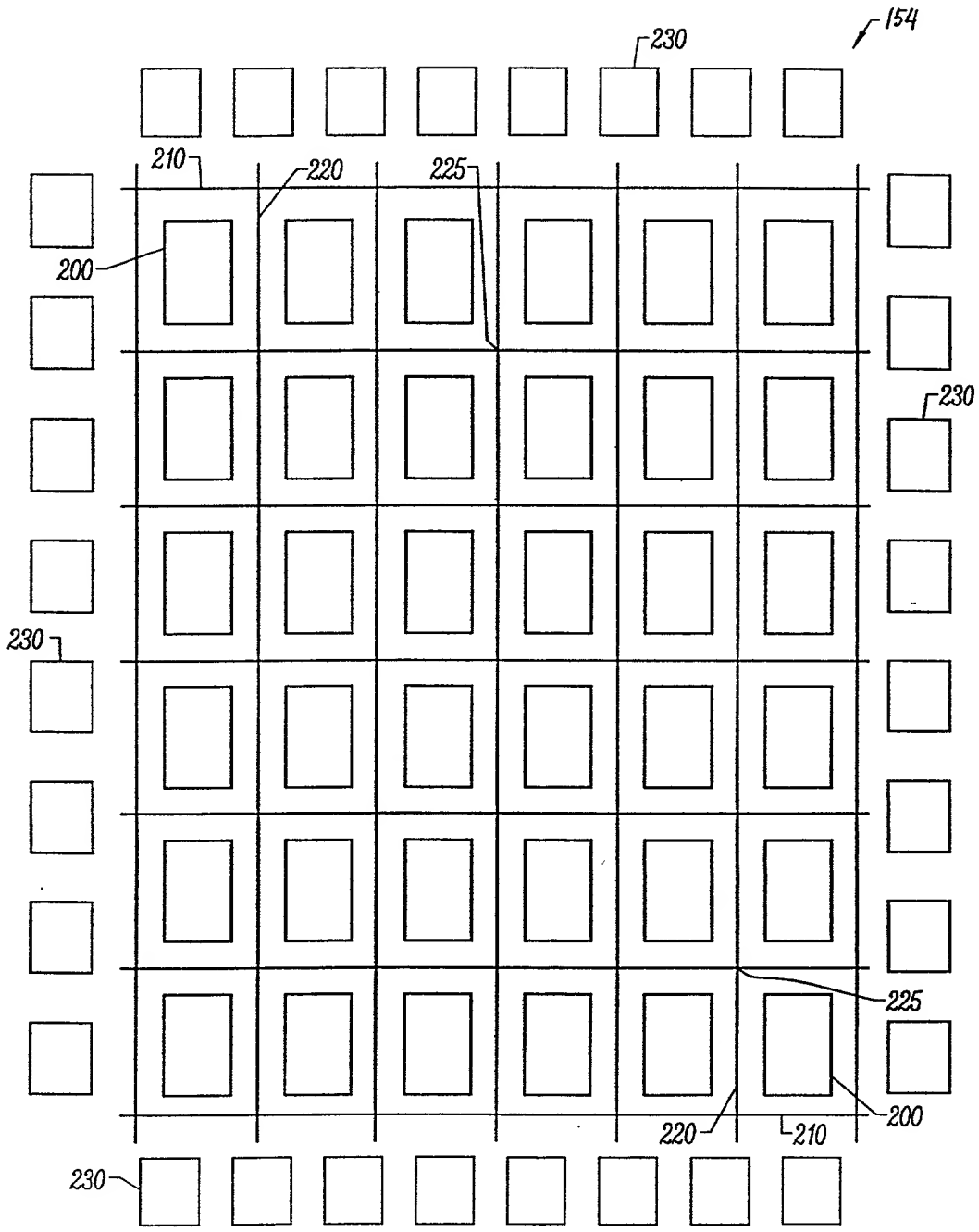


FIGURE 3

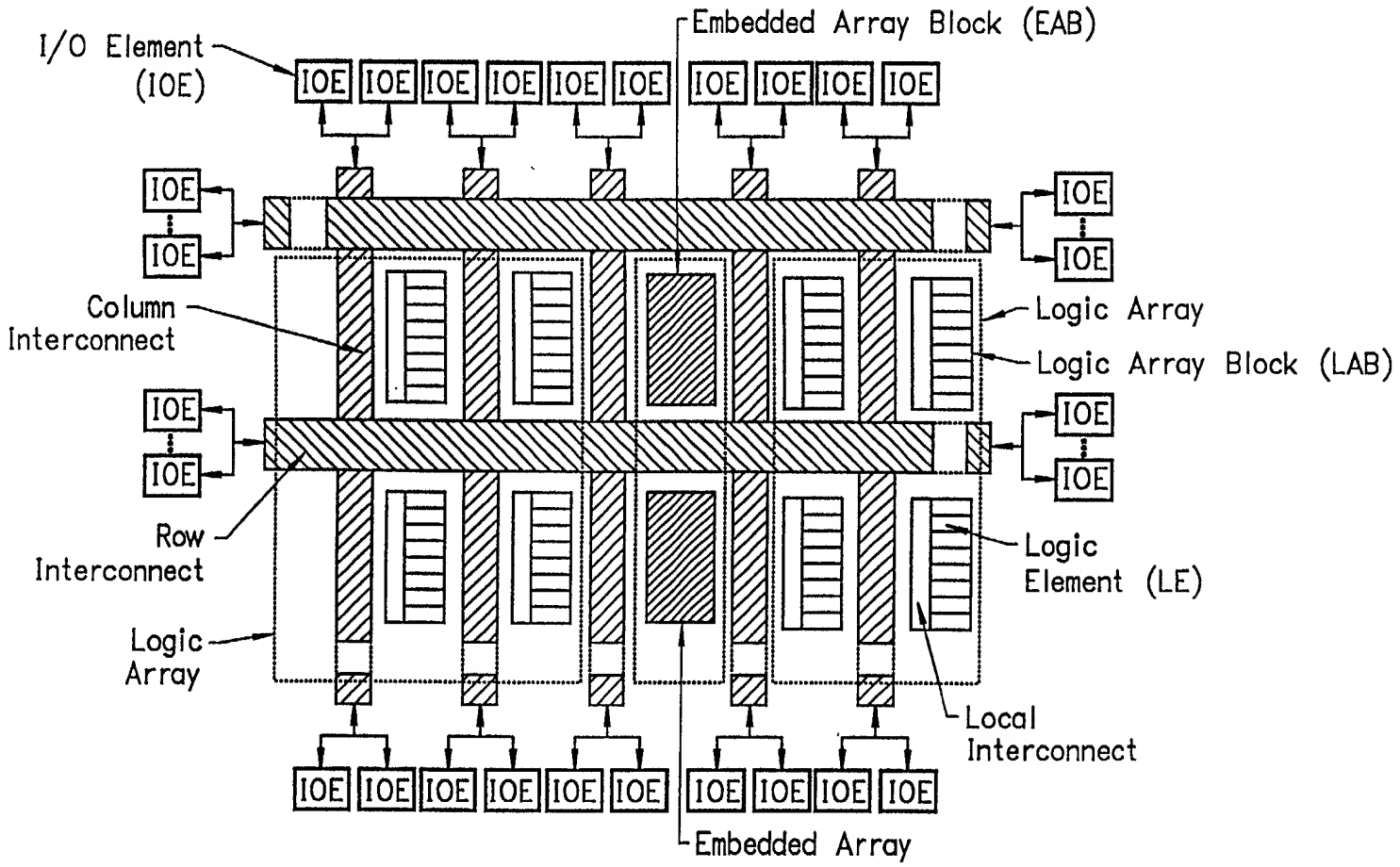


FIGURE 5

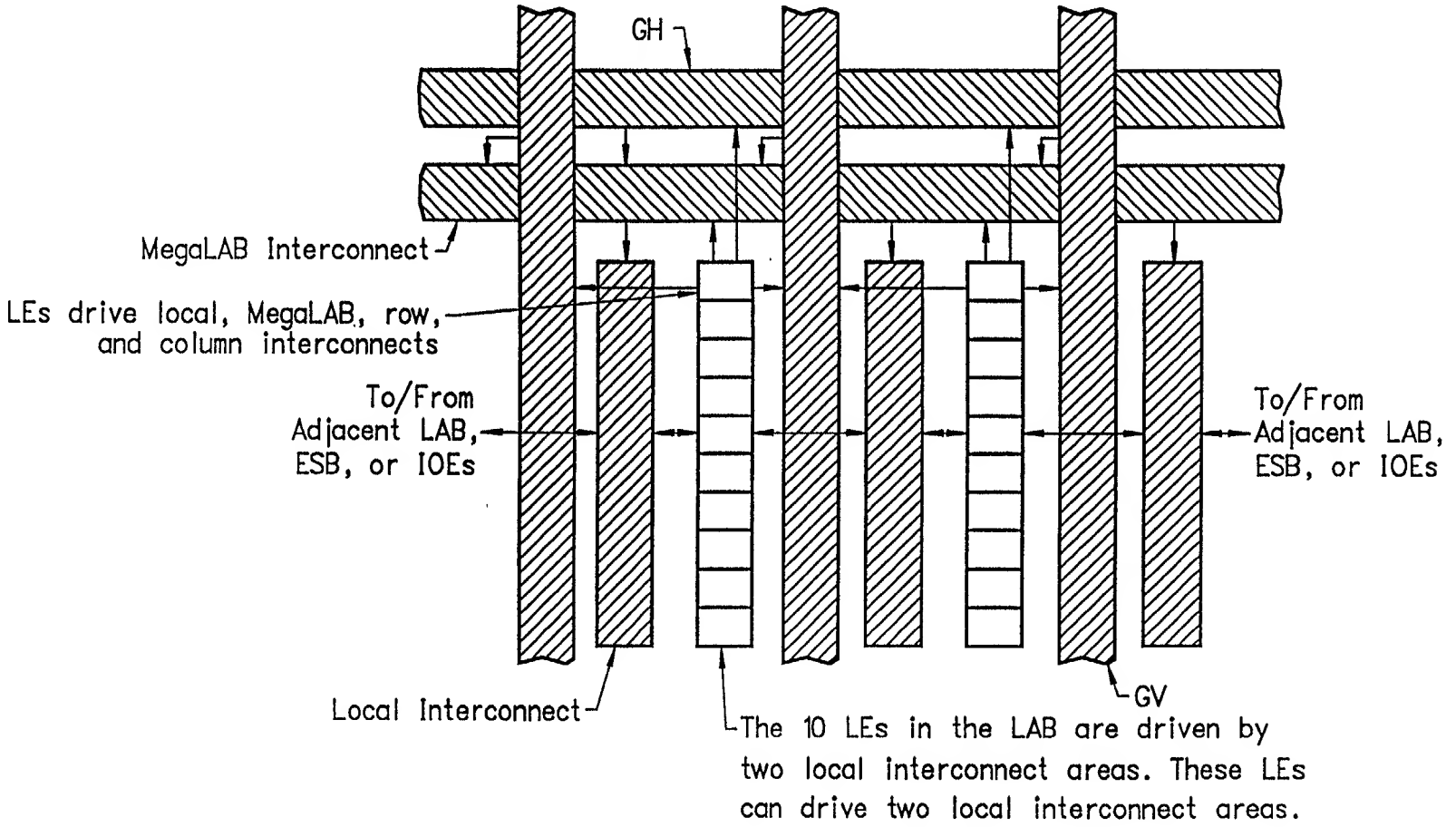


FIGURE 6

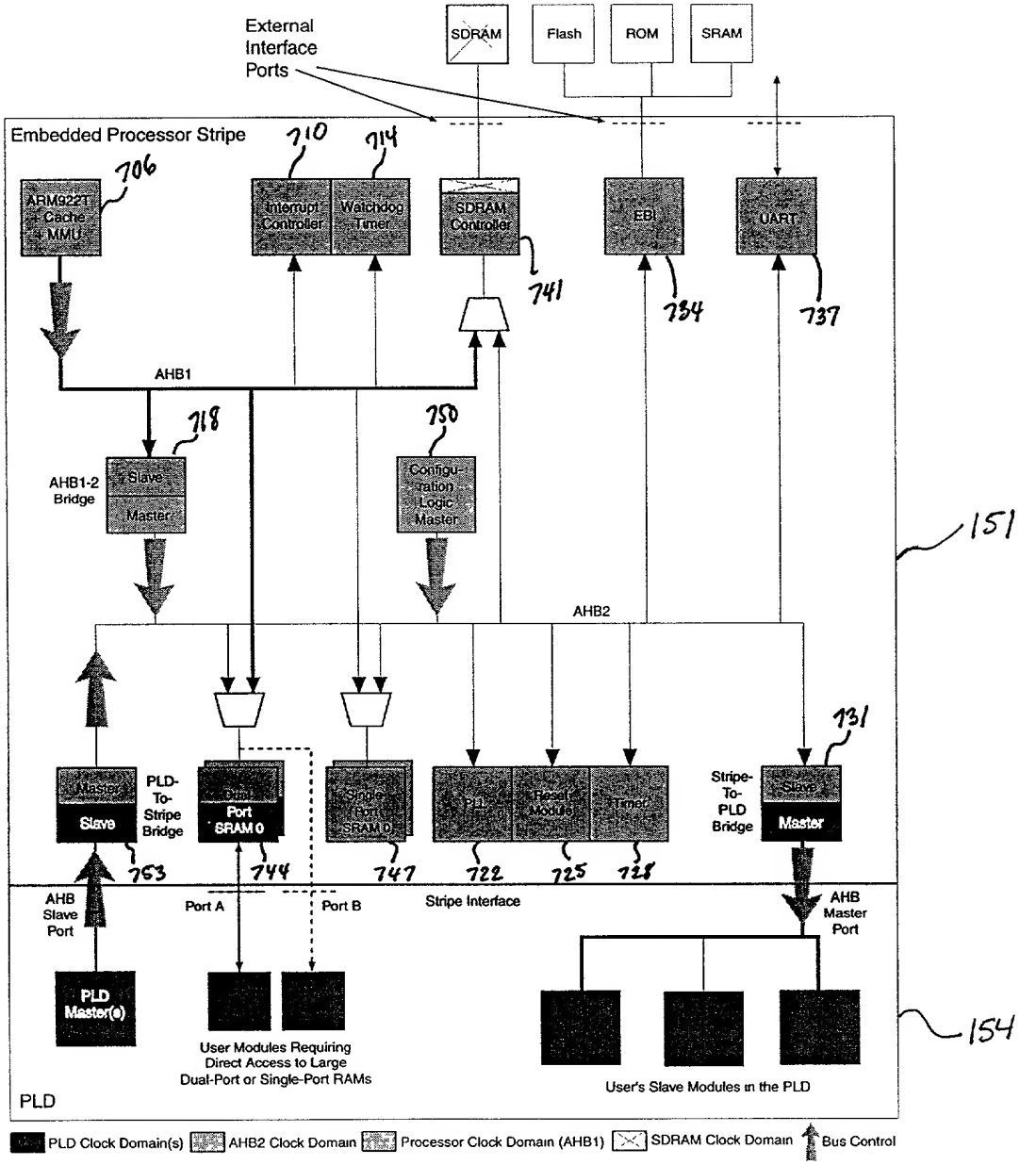

External Interface Ports
SDRAM
Flash
ROM
SRAM
Embedded Processor Stripe
710
714
706
ARM922T + Cache + MMU
Interrupt Controller
Watchdog Timer
SDRAM Controller
EBI
UART
741
734
737
AHB1
718
750
AHB1-2 Bridge
Slave
Master
Configu-ration Logic Master
151
AHB2
731
Slave
PLD-To-Stripe Bridge
Port SRAM 0
Stripe-To-PLD Bridge
Master
753
744
747
722
725
728
AHB Slave Port
Port A
Port B
Stripe Interface
AHB Master Port
PLD Master(s)
User Modules Requiring Direct Access to Large Dual-Port or Single-Port RAMs
154
User's Slave Modules in the PLD
PLD
PLD Clock Domain(s)
AHB2 Clock Domain
Processor Clock Domain (AHB1)
SDRAM Clock Domain
Bus Control

FIGURE 7

FIGURE 8

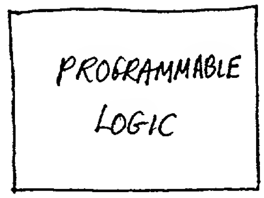


FIGURE 9

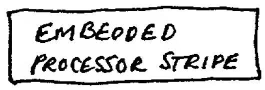


FIGURE 10

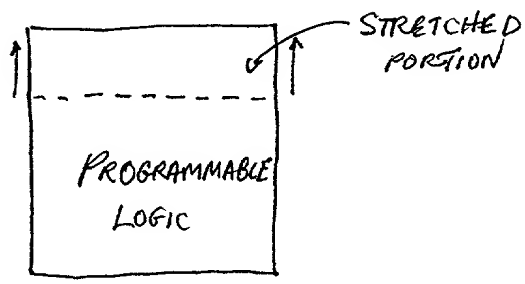
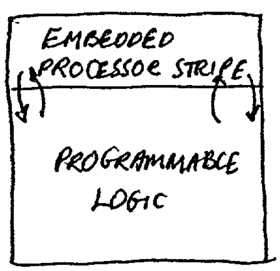


FIGURE 11



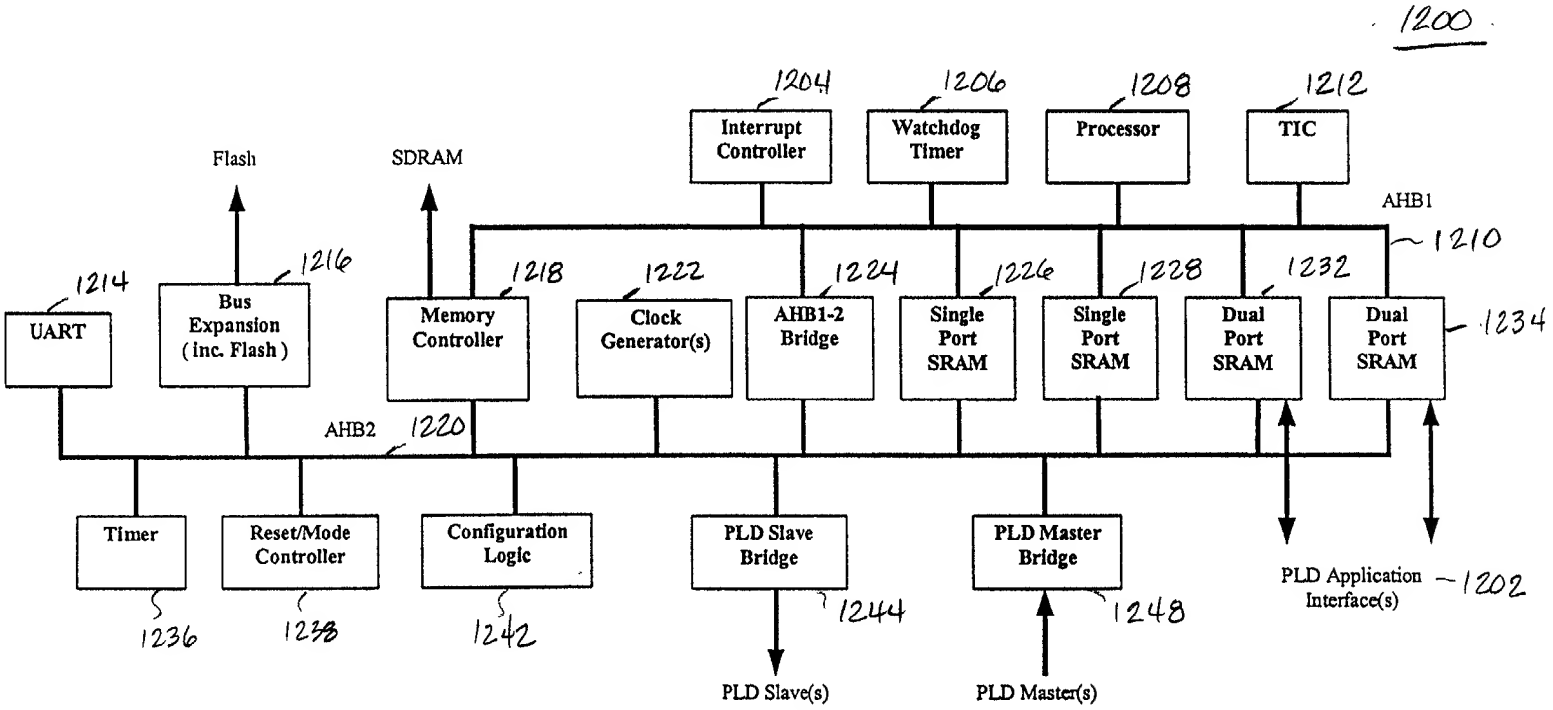


FIGURE 12

32

8K

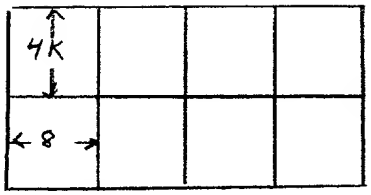


FIGURE 13A

8K x 32

16

16K

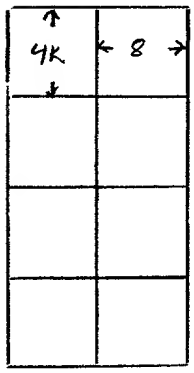


FIGURE 13B

16K x 16

8

32K

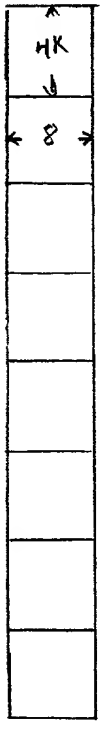


FIGURE 13C

32K x 8

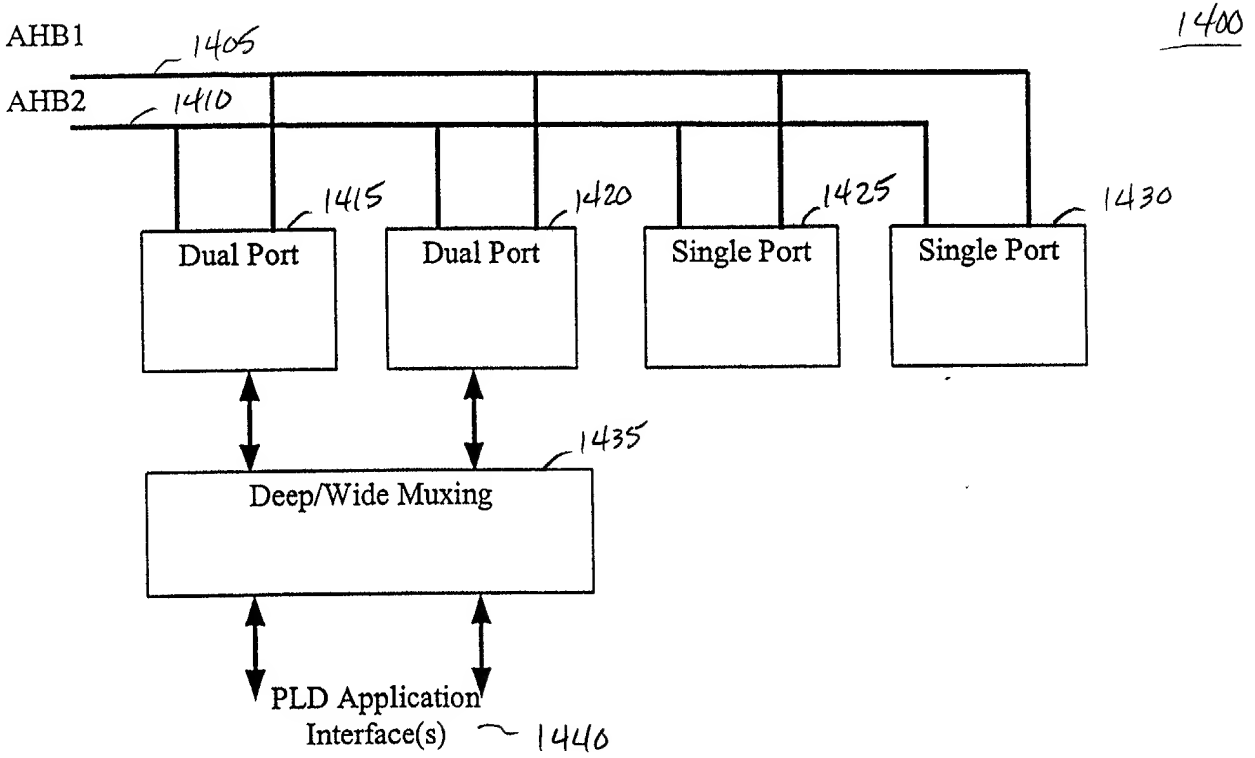


FIGURE 14

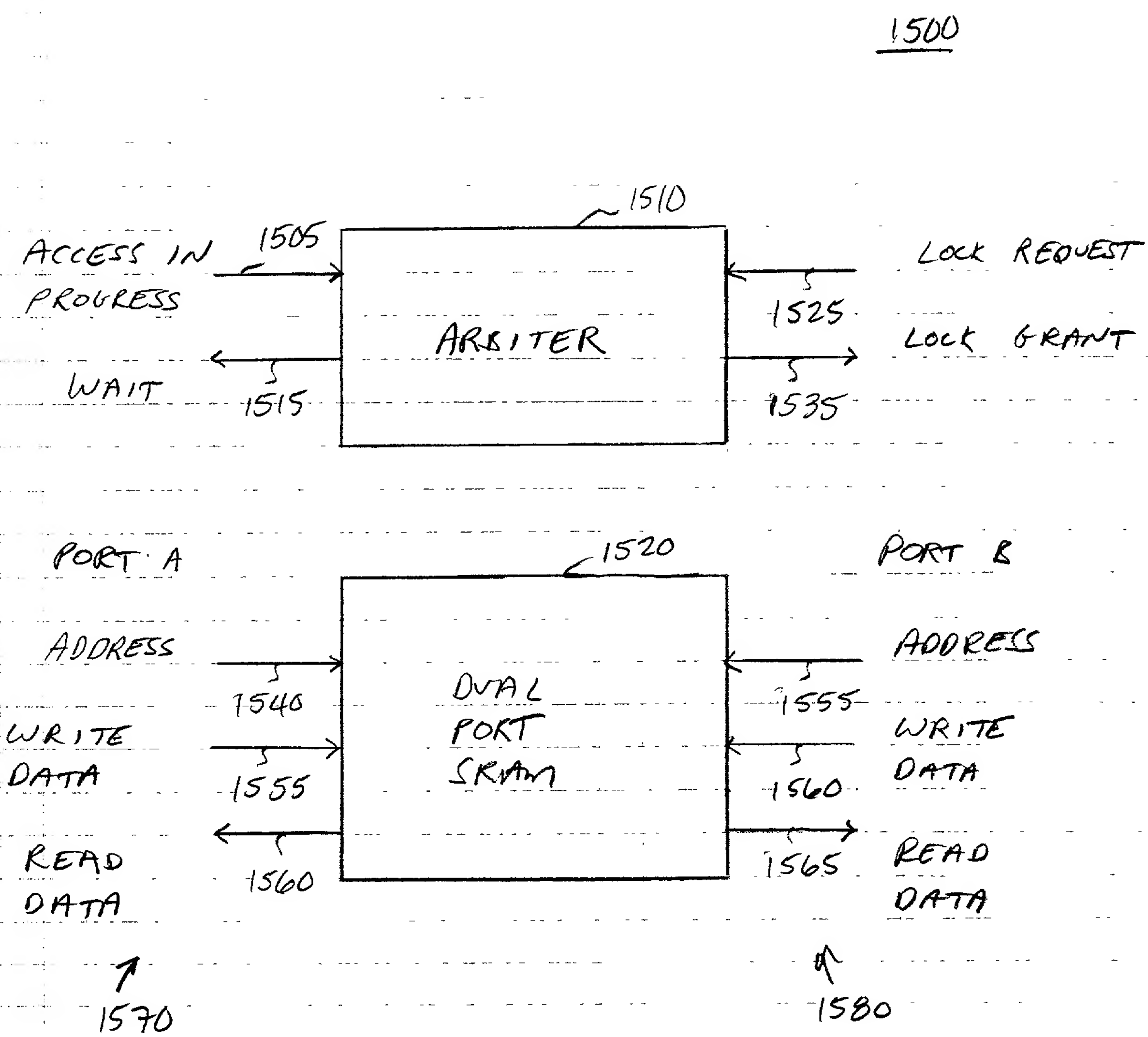

1500
1510
ACCESS IN PROGRESS
1505
WAIT
1515
ARBITER
LOCK REQUEST
1525
LOCK GRANT
1535
PORT A
1520
PORT B
ADDRESS
1540
WRITE DATA
1555
READ DATA
1560
DUAL PORT SRAM
ADDRESS
1555
WRITE DATA
1560
READ DATA
1565
1570
1580

Figure 15

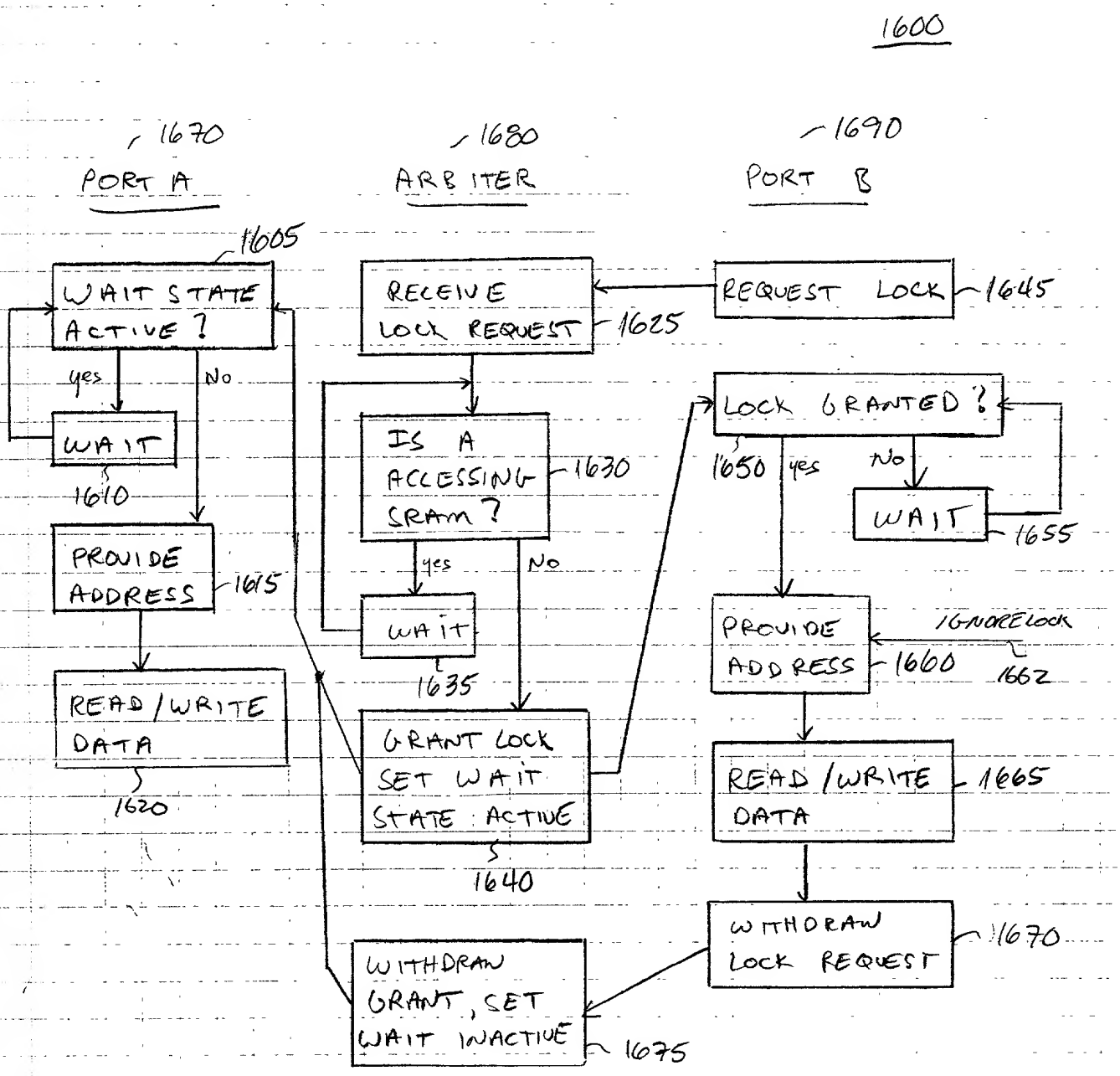

1600
1670
PORT A
1680
ARBITER
1690
PORT B
1605
WAIT STATE ACTIVE ?
yes
No
WAIT
1610
PROVIDE ADDRESS
1615
READ / WRITE DATA
1620
RECEIVE LOCK REQUEST
1625
IS A ACCESSING SRAM ?
1630
yes
No
WAIT
1635
GRANT LOCK SET WAIT STATE ACTIVE
1640
WITHDRAW GRANT, SET WAIT INACTIVE
1675
REQUEST LOCK
1645
LOCK GRANTED ?
1650
yes
No
WAIT
1655
PROVIDE ADDRESS
1660
IGNORE LOCK
1662
READ / WRITE DATA
1665
WITHDRAW LOCK REQUEST
1670

FIGURE 16

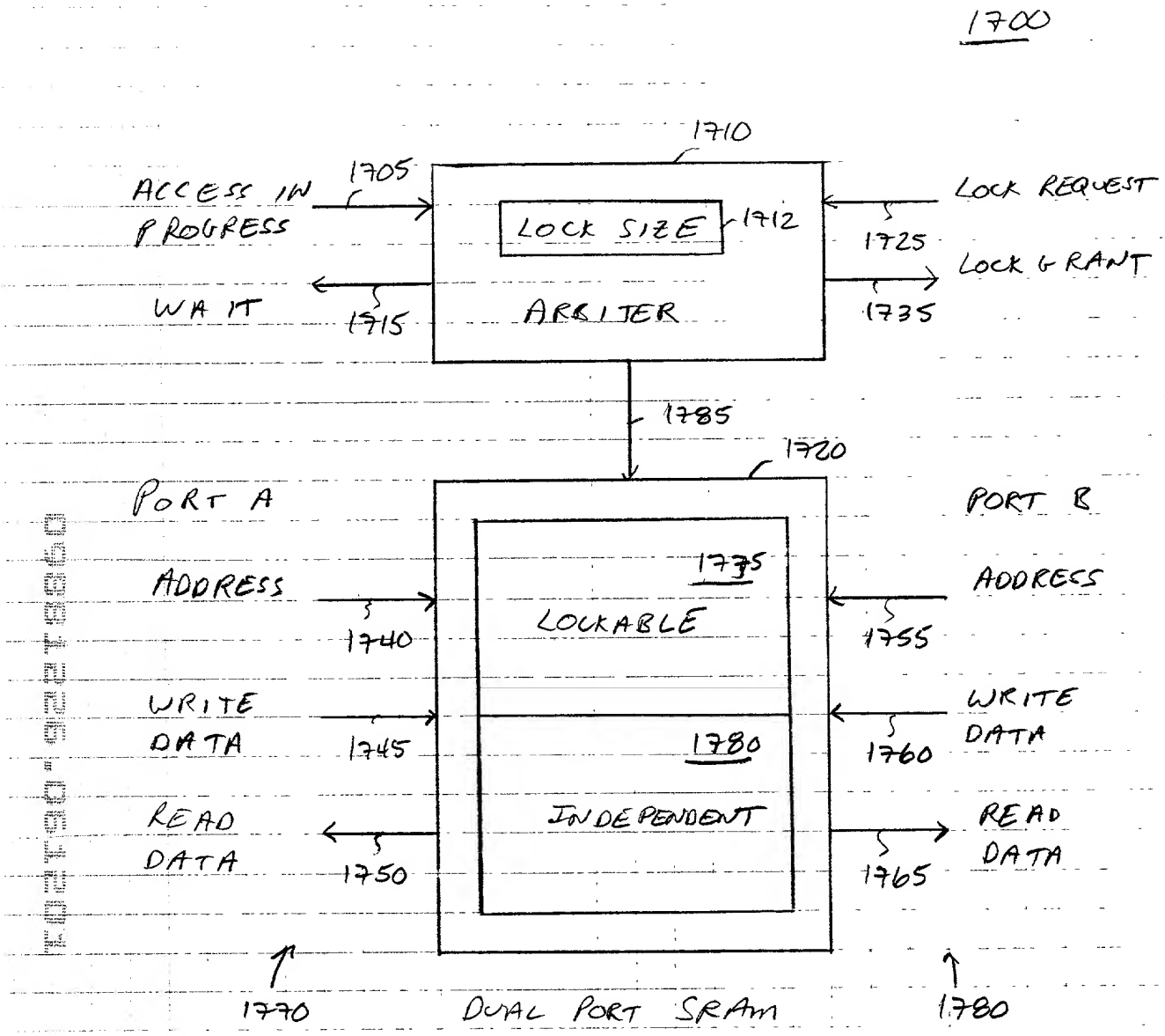

1700
1710
1705
ACCESS IN PROGRESS
LOCK SIZE
1712
LOCK REQUEST
1725
LOCK GRANT
WAIT
1715
ARBITER
1735
1785
1720
PORT A
PORT B
1775
ADDRESS
1740
LOCKABLE
ADDRESS
1755
WRITE DATA
1745
1780
WRITE DATA
1760
READ DATA
1750
INDEPENDENT
READ DATA
1765
1770
DUAL PORT SRAM
1780

FIGURE 17

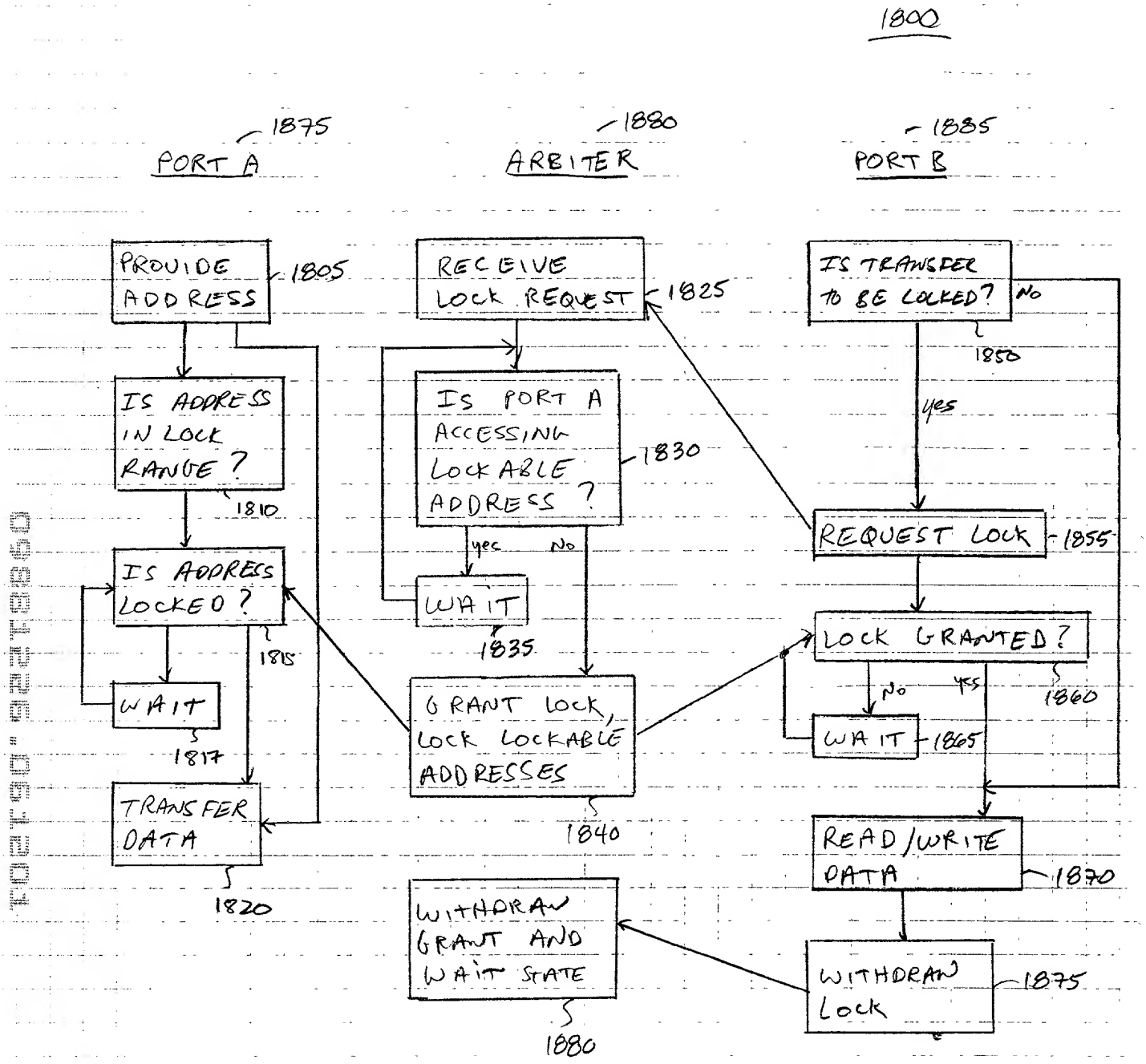

1800
1875
PORT A
1880
ARBITER
1885
PORT B
PROVIDE ADDRESS
1805
IS ADDRESS IN LOCK RANGE?
1810
IS ADDRESS LOCKED?
1815
WAIT
1817
TRANSFER DATA
1820
RECEIVE LOCK REQUEST
1825
IS PORT A ACCESSING LOCKABLE ADDRESS?
1830
yes
No
WAIT
1835
GRANT LOCK, LOCK LOCKABLE ADDRESSES
1840
WITHDRAW GRANT AND WAIT STATE
1880
IS TRANSFER TO BE LOCKED?
No
1850
yes
REQUEST LOCK
1855
LOCK GRANTED?
No
Yes
1860
WAIT
1865
READ/WRITE DATA
1870
WITHDRAW LOCK
1875

FIGURE 18

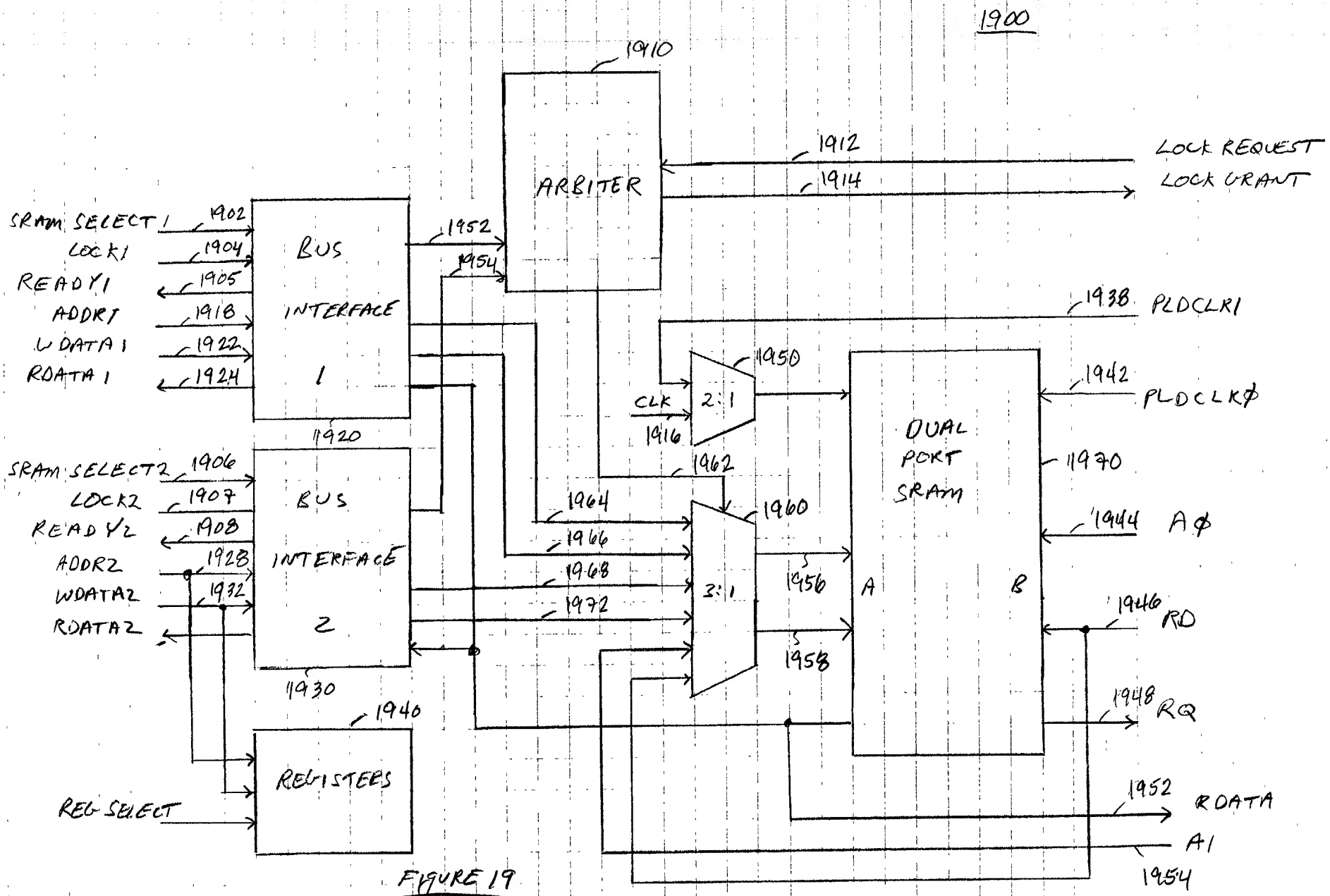


FIGURE 19

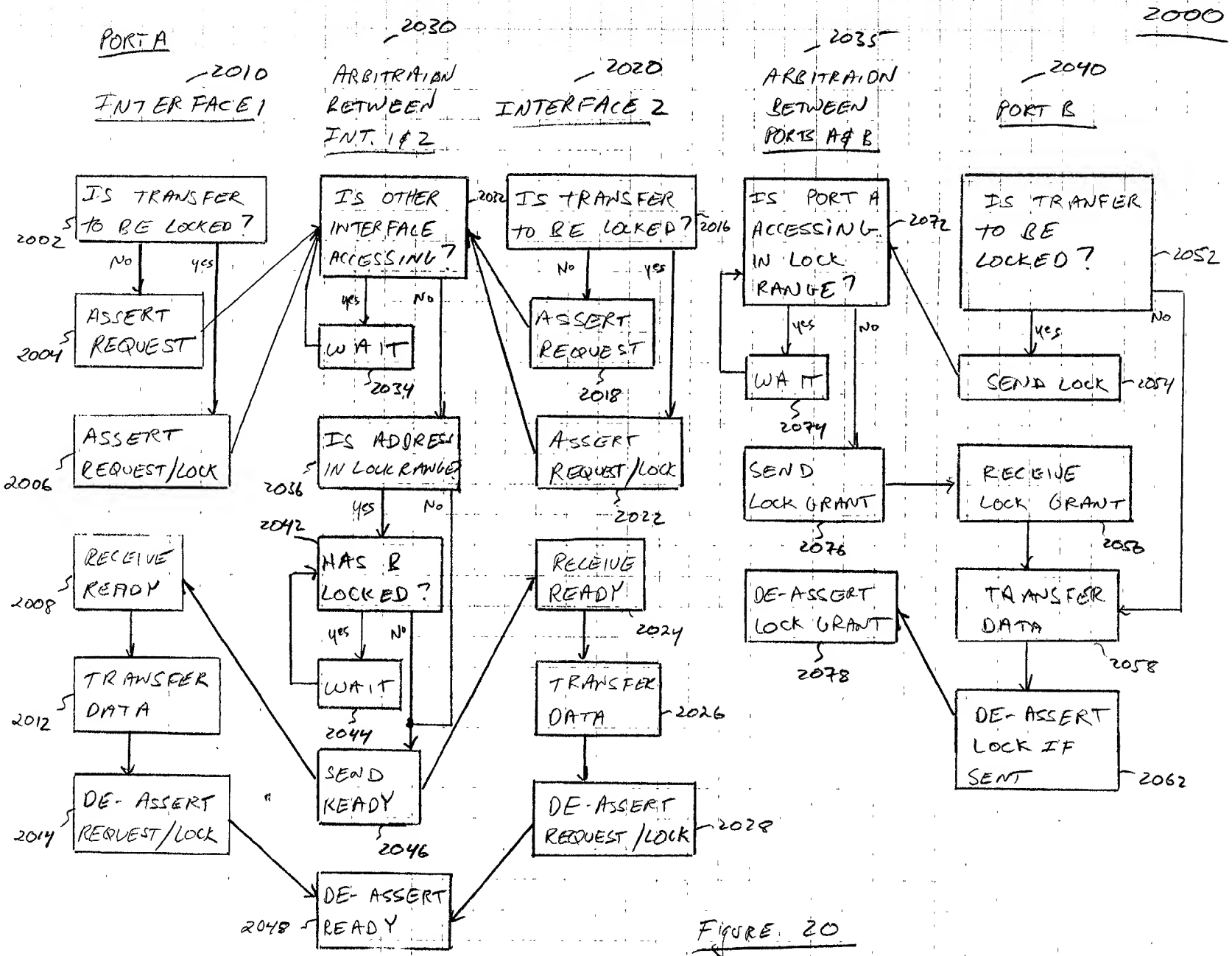


FIGURE 20

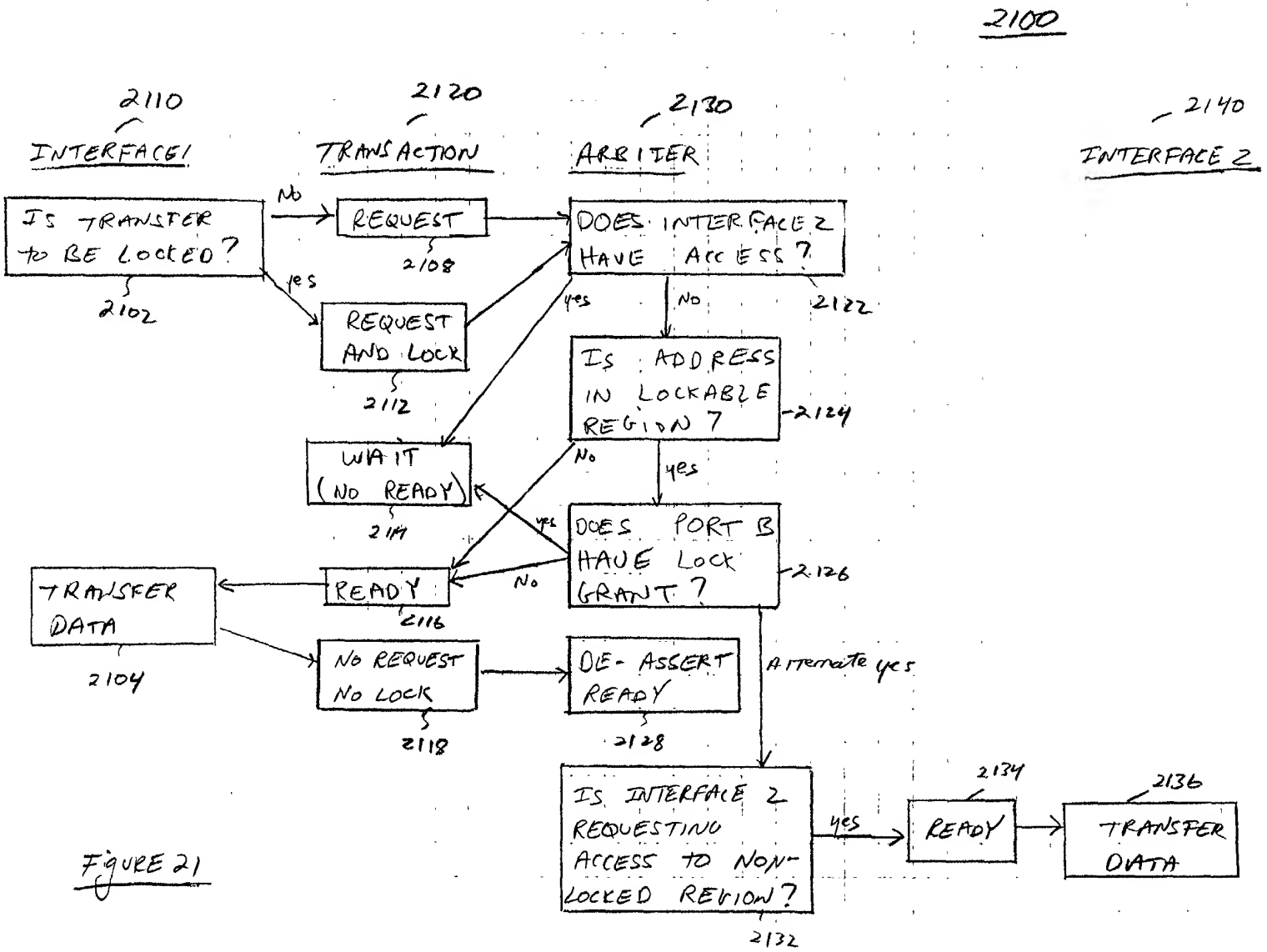

2100
2110
INTERFACE1
2120
TRANSACTION
2130
ARBITER
2140
INTERFACE 2
IS TRANSFER TO BE LOCKED?
2102
No
yes
REQUEST
2108
REQUEST AND LOCK
2112
DOES INTERFACE 2 HAVE ACCESS?
2122
yes
No
IS ADDRESS IN LOCKABLE REGION?
2124
No
yes
WAIT (NO READY)
2114
DOES PORT B HAVE LOCK GRANT?
2126
yes
No
READY
2116
TRANSFER DATA
2104
NO REQUEST NO LOCK
2118
DE-ASSERT READY
2128
Alternate yes
IS INTERFACE 2 REQUESTING ACCESS TO NON-LOCKED REGION?
2132
yes
2134
READY
2136
TRANSFER DATA

Figure 21

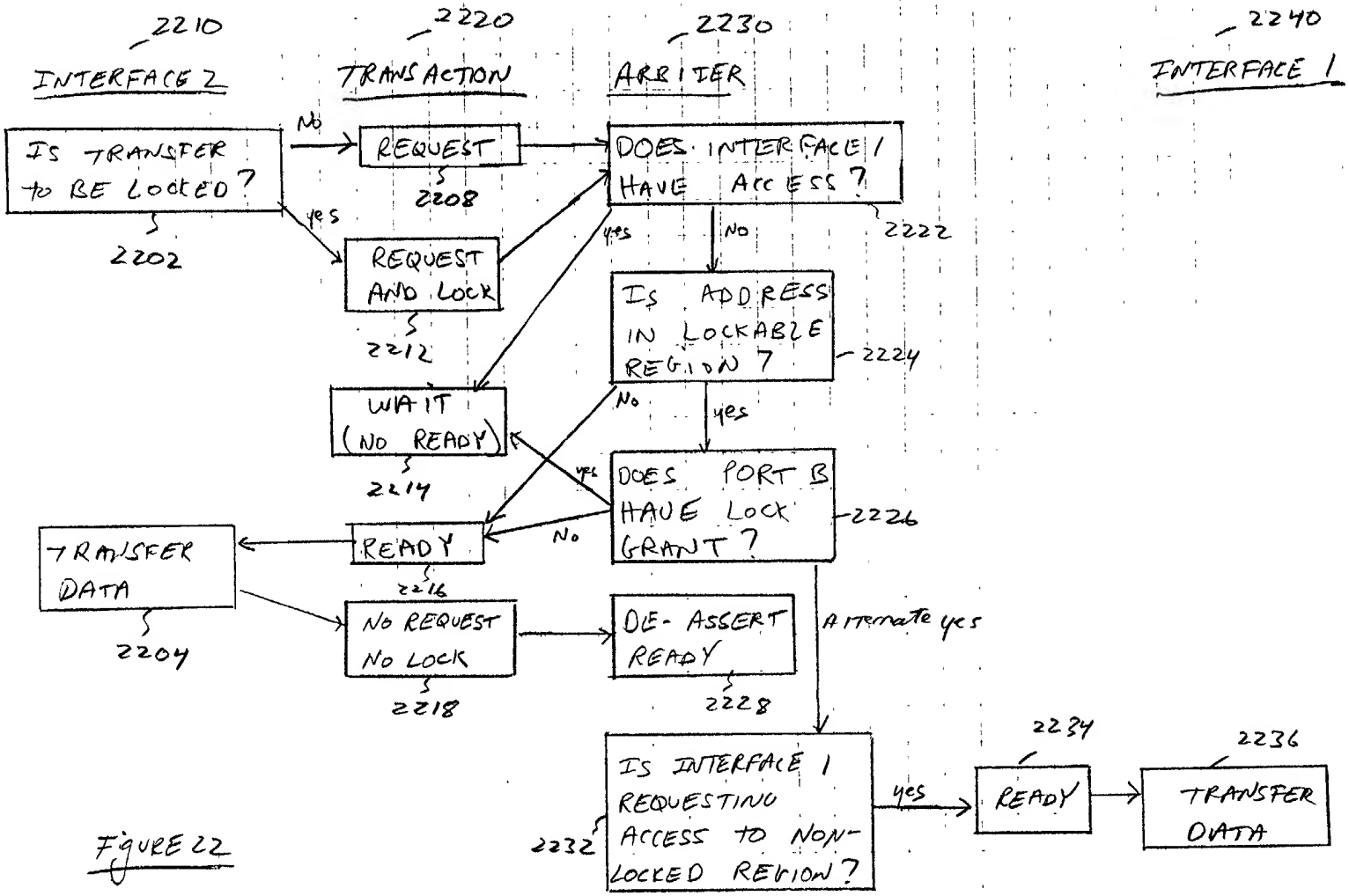


Figure 22

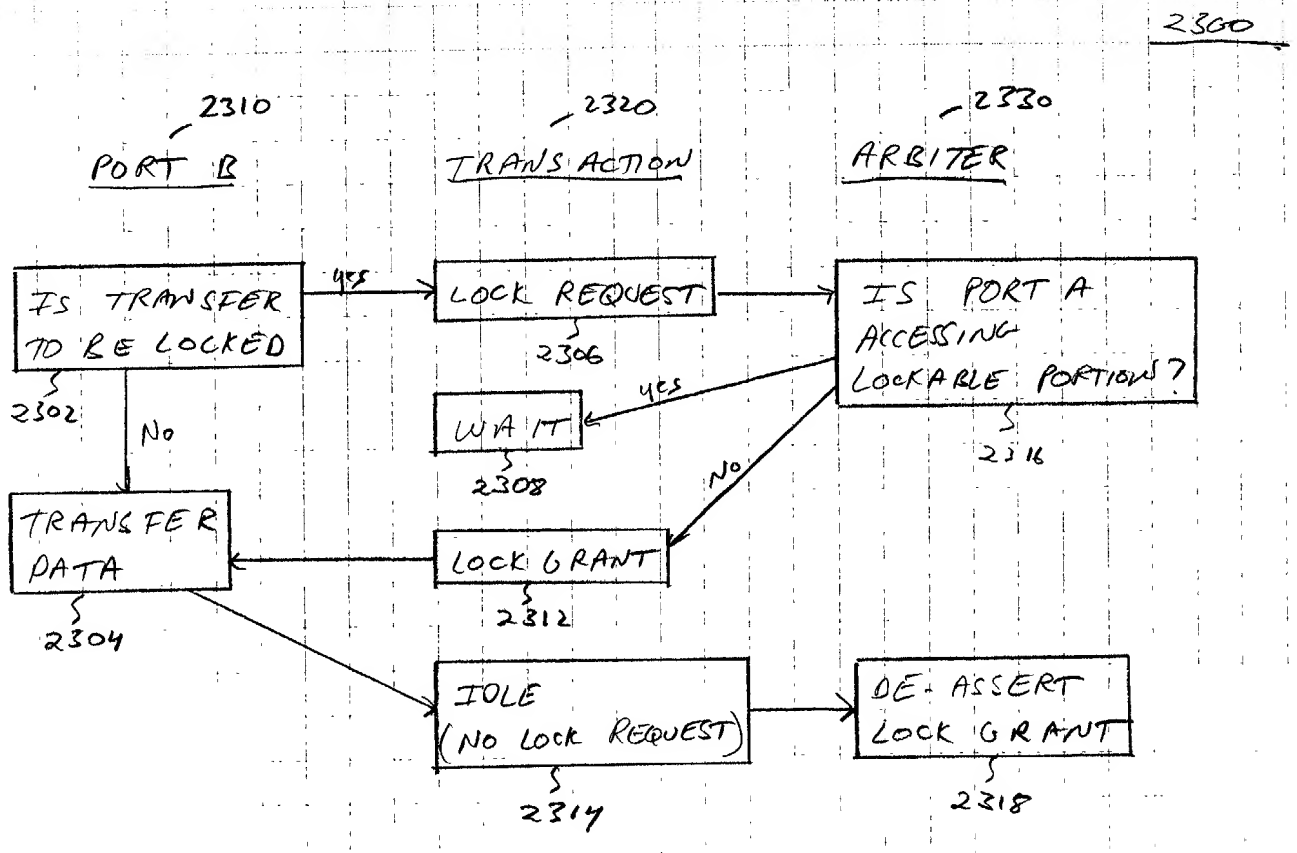


FIGURE 23

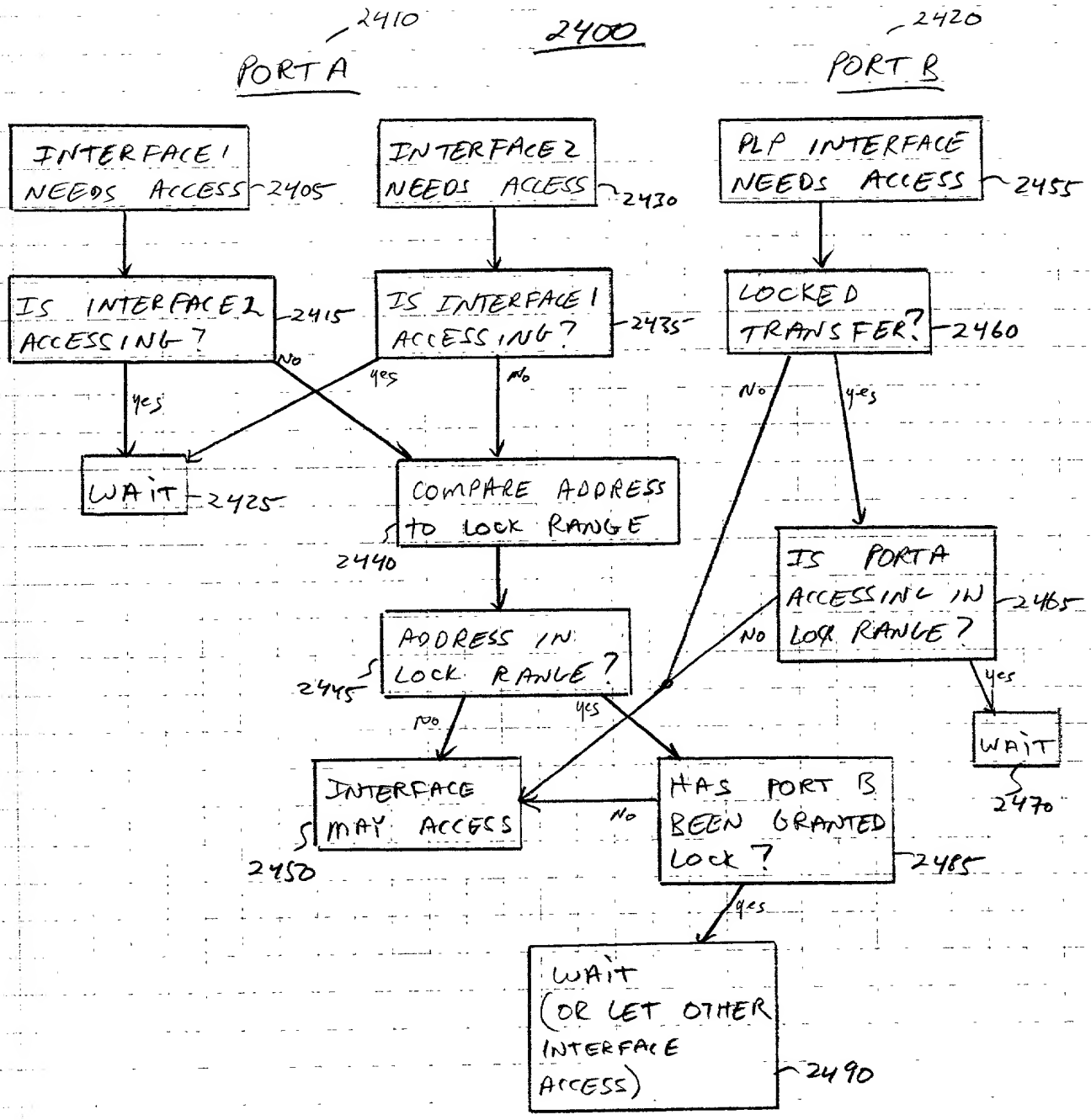

2400
PORT A
2410
PORT B
2420
INTERFACE 1 NEEDS ACCESS
2405
INTERFACE 2 NEEDS ACCESS
2430
PLP INTERFACE NEEDS ACCESS
2455
IS INTERFACE 2 ACCESSING?
2415
IS INTERFACE 1 ACCESSING?
2435
LOCKED TRANSFER?
2460
No
yes
yes
No
No
yes
WAIT
2425
COMPARE ADDRESS TO LOCK RANGE
2440
IS PORT A ACCESSING IN LOCK RANGE?
2465
No
yes
ADDRESS IN LOCK RANGE?
2445
No
yes
WAIT
2470
INTERFACE MAY ACCESS
2450
No
HAS PORT B BEEN GRANTED LOCK?
2485
yes
WAIT (OR LET OTHER INTERFACE ACCESS)
2490

FIGURE 24

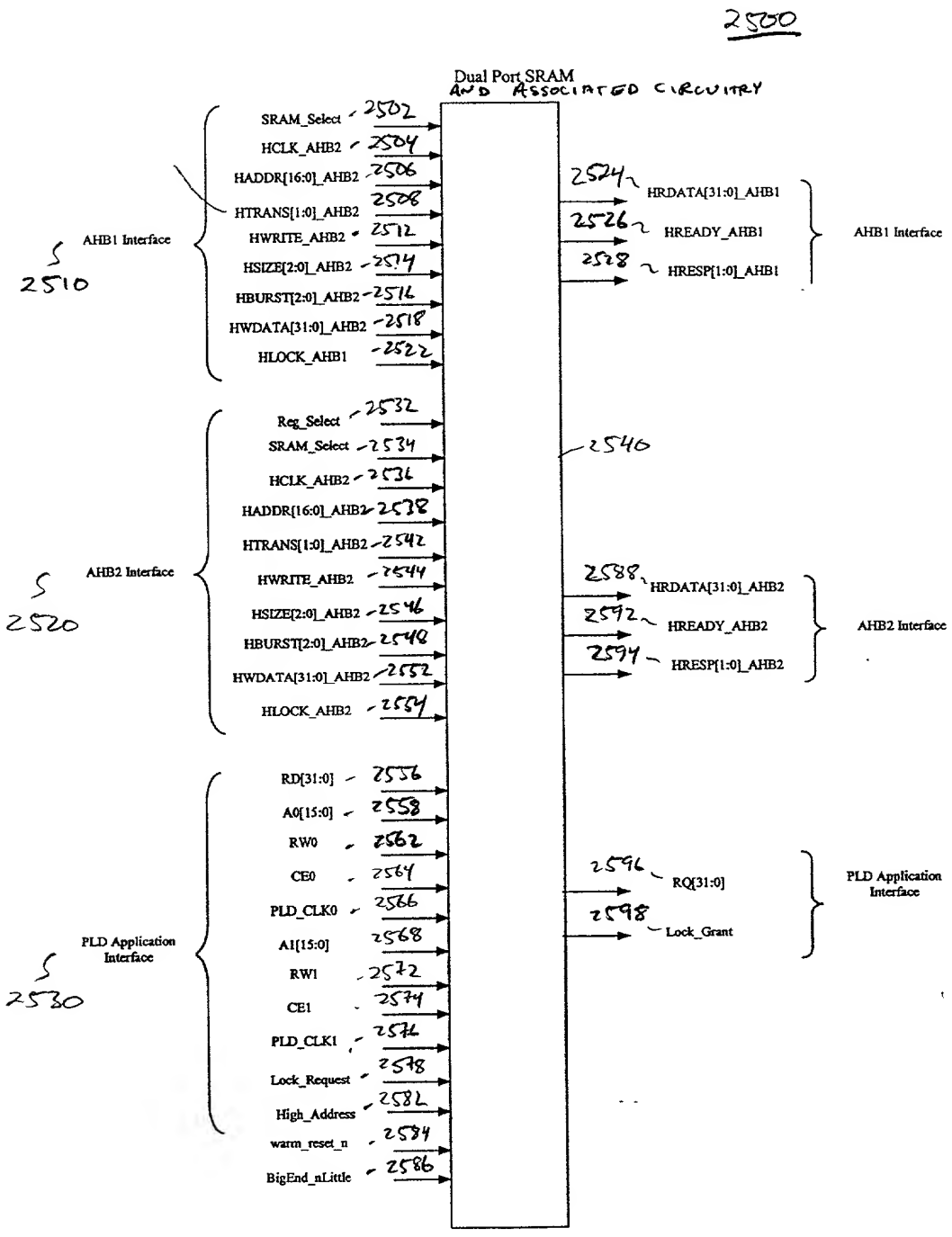

2500
Dual Port SRAM
AND ASSOCIATED CIRCUITRY
AHB1 Interface
2510
SRAM_Select 2502
HCLK_AHB2 2504
HADDR[16:0]_AHB2 2506
HTRANS[1:0]_AHB2 2508
HWRITE_AHB2 2512
HSIZE[2:0]_AHB2 2514
HBURST[2:0]_AHB2 2516
HWDATA[31:0]_AHB2 2518
HLOCK_AHB1 2522
2524 HRDATA[31:0]_AHB1
2526 HREADY_AHB1
2528 HRESP[1:0]_AHB1
AHB1 Interface
AHB2 Interface
2520
Reg_Select 2532
SRAM_Select 2534
HCLK_AHB2 2536
HADDR[16:0]_AHB2 2538
HTRANS[1:0]_AHB2 2542
HWRITE_AHB2 2544
HSIZE[2:0]_AHB2 2546
HBURST[2:0]_AHB2 2548
HWDATA[31:0]_AHB2 2552
HLOCK_AHB2 2554
2540
2588 HRDATA[31:0]_AHB2
2592 HREADY_AHB2
2594 HRESP[1:0]_AHB2
AHB2 Interface
PLD Application Interface
2530
RD[31:0] 2556
A0[15:0] 2558
RW0 2562
CE0 2564
PLD_CLK0 2566
A1[15:0] 2568
RW1 2572
CE1 2574
PLD_CLK1 2576
Lock_Request 2578
High_Address 2582
warm_reset_n 2584
BigEnd_nLittle 2586
2596 RQ[31:0]
2598 Lock_Grant
PLD Application Interface

FIGURE 25